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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,699	11/30/2001	Hiroshi Sakurai	NEG-234US	3647

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EXAMINER
NGUYEN, HOAN C

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/996,699	SAKURAI ET AL.
	Examiner	Art Unit
	HOAN C. NGUYEN	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7 and 8* is/are pending in the application.

4a) Of the above claim(s) *6 and 9-16* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Species A in Paper No. 7 (1-8) is acknowledged.

Applicant's arguments regarding the restriction requirement have been considered; however, the traversal was on the grounds that there is no serious burden on the Examiner in examining all of claims 1-16 together. This is not found persuasive since a reflection type liquid crystal display device (claims 9-16) can be produced by photolithography with photo-sensitive layer and etching process while a process for producing a reflection type liquid crystal display device (claim 1-8) with mask to form source/drain electrode and laser to form an opening for contact hole.

Therefore, the requirement is deemed proper and is considered to be final.

However, claim 6 read on nonelected species B drawn to manufacture the protective circuit, Figures 9-16.

Claims 6 and 9-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions and species, there being no allowable generic or linking claim.

Claims 1-5 and 7-8 are considered to be in the elected species A.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of "first, second, third and fourth masks" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: the inconsistent languages appear in specification. For examples:

- Layers 22 and 23 assign to be drain line and source line in paragraphs 49, 51, 56-58 and claims 1, 2 and 5. However, layers 22 and 23 assign to be drain electrode and source electrode in paragraphs 66, 68-70, 78, 86, 92 and 93.
- "Gate wiring" means "**gate electrode**" citing in "forming a thin film transistor region and gate wiring by using a second mask" of the abstract, paragraphs 11, 12, 15, 16, 19, 57, 58 and claims 1, 2 and 5. However, "gate wiring" means "**gate bus wiring**" citing in "forming said gate wiring on said insulating substrate having said capacitor electrode" of claim 5 and "a capacitor electrode is formed when said source/drain wiring is formed, in that said gate wiring is formed on said insulating substrate including said capacitor electrode" of paragraph 15.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-5 and 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1:

- "source/drain wiring" should be "source/drain electrode" or "gate/drain wire pattern"?
- What does applicant intend to cite "depositing a silicon layer, gate insulating film and gate electrode layer in this order to form a thin film transistor region and a gate wiring (gate electrode?)"? Is a gate wiring also formed by this order of "a silicon layer, gate insulating film and gate electrode layer". Fig. 3 shows gate line 51 connected to gate electrode layer 52, which is formed on gate insulating layer 40 and silicon layer 30.
- Applicant cites "depositing a passivation film on said insulating substrate having said source/drain wiring, said thin film transistor region and said gate wiring formed thereon to form an opening." How does "depositing a passivation film" form an opening with third mask? What is third mask like? The type of mask and process to form an opening do not disclose in the specification.

- Applicant cites "said thin film transistor region and said gate wiring formed thereon to form an opening for the transistor through said passivation film at a predetermined position on said source wiring." How can the thin film transistor region and the gate wiring form an opening for (contact hole?) the transistor?
- Applicant cites "forming a rough surface of said interlayer insulating film to form an opening for the transistor through said interlayer insulating film." How can "forming a rough surface of said interlayer insulating film" form "an opening for the transistor (contact hole?) through said interlayer insulating film."

In claim 2:

- The same problems stated in claim 1.
- Applicant cites "forming an opening for (contact hole?) transistor through said passivation film in a position corresponding to the opening for the transistor in said interlayer insulating film by using said interlayer insulating film as a mask." How is this procedure performed?

Specification also fails to disclose **the process** to form the opening through passivation film by using the interlayer insulating film as a mask. Please provide **Drawings** of the process of forming the opening through passivation film by using the interlayer insulating film as a mask.

In claim 5:

- The same problems stated in claims 1 and 2.

- Applicant cites "forming said gate wiring (gate bus wiring?) on said insulating substrate having said capacitor electrode formed when forming said thin film transistor region and said gate wiring (electrode?) are formed (?)" Is this means "forming said gate wiring when said thin film transistor region and said gate wiring are formed"? How can it be?

In claim 8:

- The same problems stated in claims 1 and 2.
- "treating at least said source/drain wiring with PH_{33}" should be "treating at least said source/drain wiring with PH_3". What is PH_3? Is PH_3 Phosphine for making the ohmic contact on the drain/source electrodes?

Claims 3-4 and 7 are rejected since they depend on infinite claim.

Applicants are advised to correct though the specification and claims for consistent terminology.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (US5907008A) in view of Katsuya et al. (US6081310A).

Nakano et al. teach (Fig. 6) a process for producing a reflection type liquid crystal display device comprising the steps of:

(a) depositing a low resistance metal layer 34/35a on an insulating substrate to form a source/drain electrode by using a first mask;

(b) depositing a silicon layer 38, gate insulating film 40 and gate electrode layer 5a on said insulating substrate having said source/drain electrode pattern formed thereon in this order to form a thin film transistor region and a gate wiring by using a second mask;

(c) depositing a passivation film 41 on said insulating substrate having said source/drain wiring, said thin film transistor region and said gate wiring formed thereon to form an opening for contact hole through said passivation film at a predetermined position on said source wiring by using a third mask;

(d) depositing an interlayer insulating film 43 on said passivation film, forming a rough surface of said interlayer insulating film to form an opening for the contact hole through said interlayer insulating film at a position corresponding to the opening formed in said passivation film by using a fourth mask;

wherein treating at least said source/drain electrode with phosphine (PH_3) after said source/drain wiring has been formed and prior to successive deposition of said silicon layer, gate insulating film and gate electrode layer for forming an ohmic contact at the contacting portions according to claim 8.

However, Nakano et al. fail to disclose (e) depositing a reflective metal over the rough surface of said interlayer insulating film to form by using a fifth mask a reflection electrode being extended and electrically connected to said source wiring through the openings for the transistor in said passivation film and said interlayer insulating film.

Katsuya et al. teach (Fig. 7) depositing a reflective metal over the rough surface of said interlayer insulating film 12 to form by using a mask a reflection electrode being extended and electrically connected to said source wiring through the openings for the cotact hole in said passivation film and said interlayer insulating film for diffusing light.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a process for producing a reflection type liquid crystal display device as Nakano et al. with depositing a reflective metal over the rough surface of said interlayer insulating film 12 to form by using a mask a reflection electrode being extended and electrically connected to said source wiring through the openings for the contact hole in said passivation film and said interlayer insulating film for diffusing light.

3. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (US5907008A) in view of Katsuya et al. (US6081310A) as applied to claims 1, 2 and 8 above, and further in view of SUGITA et al. (US20030022071A1).

SUGITA et al. teach (Fig. 5) the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by halftone exposure or two-times exposure, wherein the formation of the rough surface of said interlayer

insulating film and the opening for the transistor is conducted by using an exposure mask having transmissivity being controlled for carrying out overlay printing of a micro-line pattern.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a process for producing a reflection type liquid crystal display device as Nakano et al. with the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by halftone exposure or two-times exposure, wherein the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by using an exposure mask having transmissivity being controlled for carrying out overlay printing of a micro-line pattern.

Allowable Subject Matter

Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: there is no prior art teaches a process for producing a reflection type liquid crystal display device shown in Figs. 8a-e comprising the steps of:

- forming sequentially silicon layer 30, gate insulating film40 and gate lines 51 on a storage capacitor electrode 24;

- forming the reflection electrode 72 connected with the storage capacitance by contact hole 64 through passivation film 61 and interlayer insulating film 62.

wherein a storage capacitor electrode 24 is formed at the same time with the source/drain electrodes;

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Katayama (US6100947A) discloses (Fig. 2A) a reflective liquid crystal panel with capacitor electrode forming same time with gate electrode and connecting to pixel electrode.

Jung et al. (US6317173B1) disclose a liquid crystal display with capacitor electrode forming same time with gate electrode.

Jang (US5834328A) discloses a liquid crystal display with capacitor electrode forming same time with gate electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (703) 306-0472. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0530.

HOAN C. NGUYEN
Examiner
Art Unit 2871

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August 8, 2003

TOAN TON
PRIMARY EXAMINER